

Foxconn Tsingtao

Fab :A

AMD RX780&SB700 Chipset for AMD AM2+ CPU

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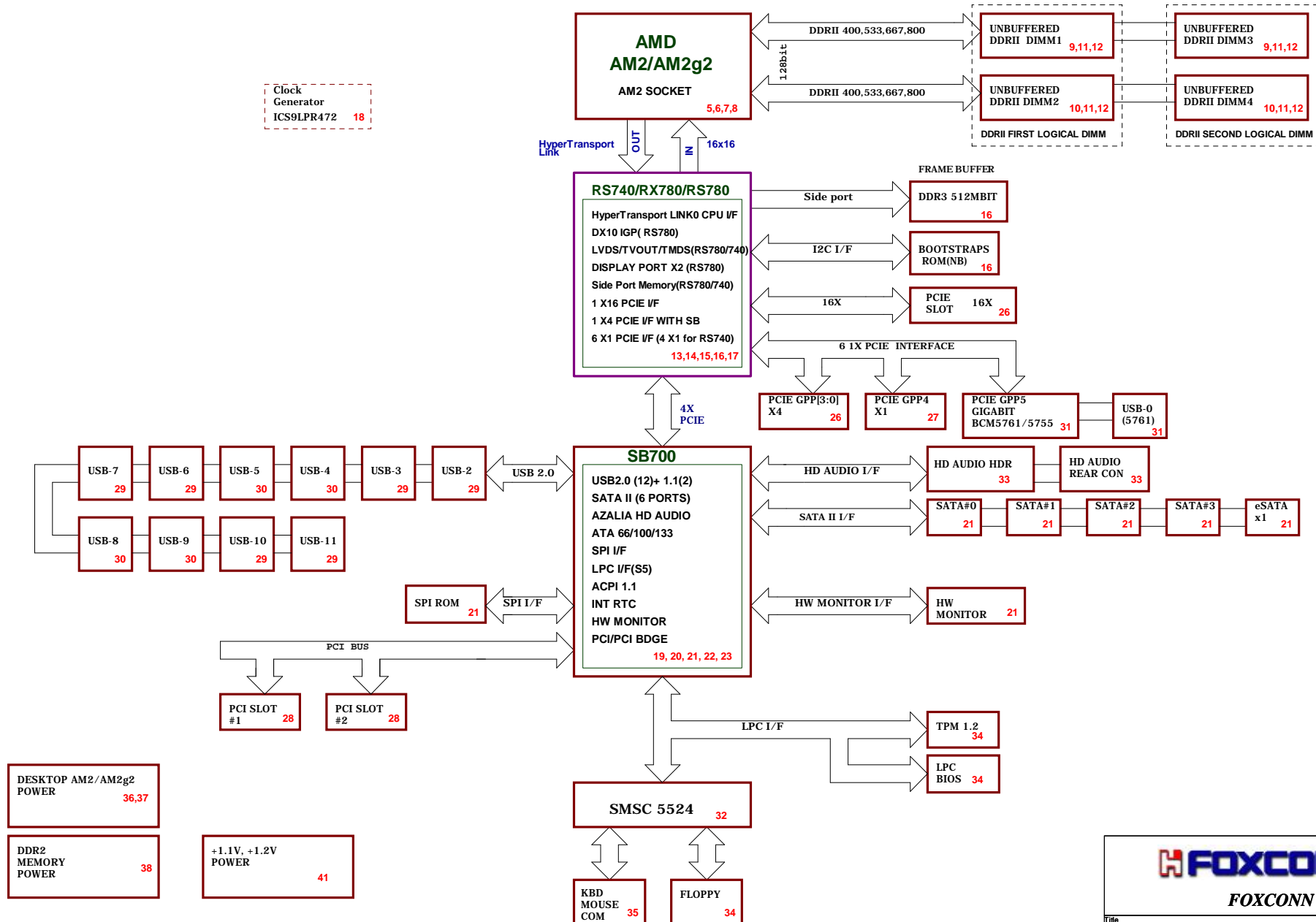
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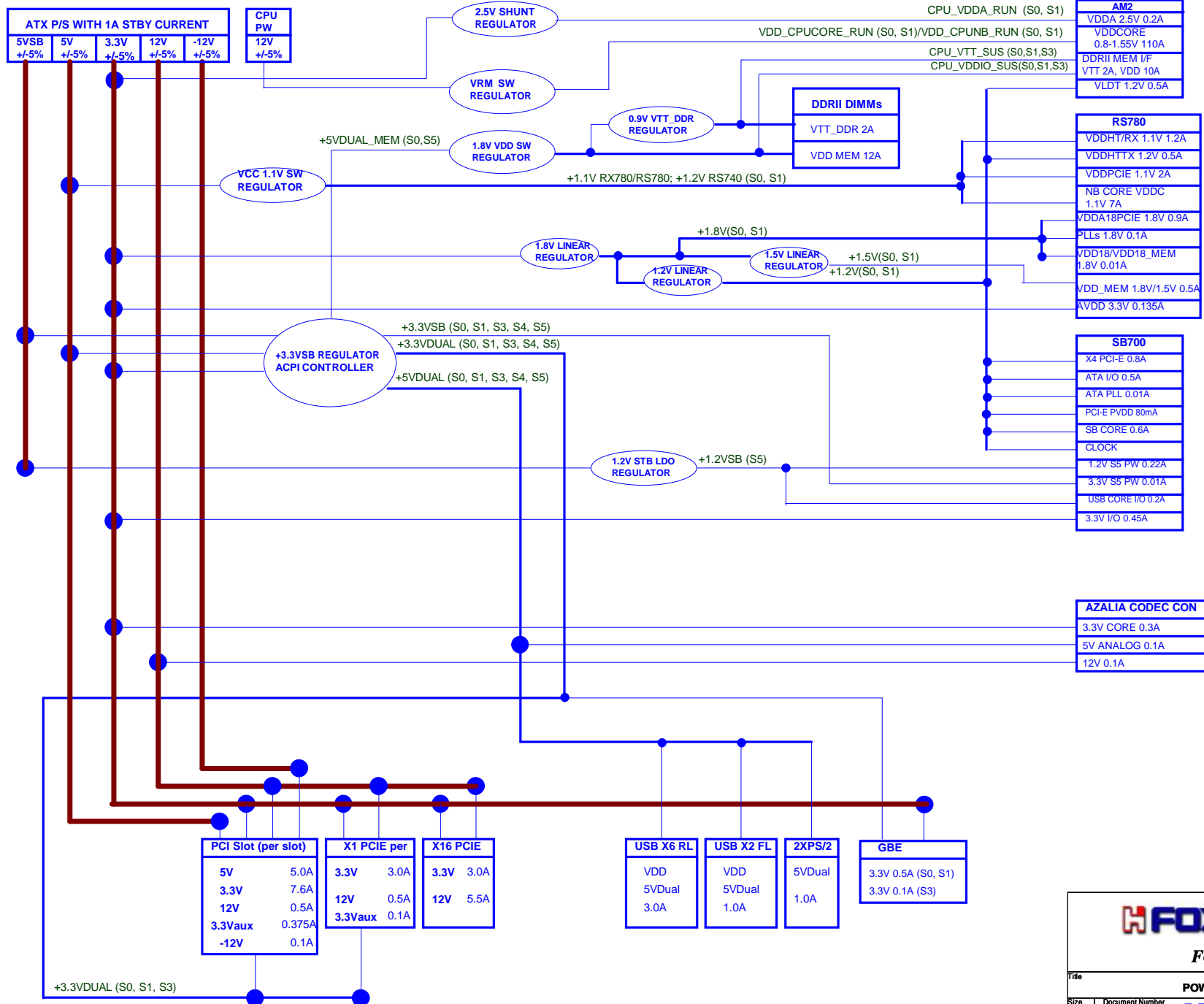
RS740/RX780/RS780 + SB700



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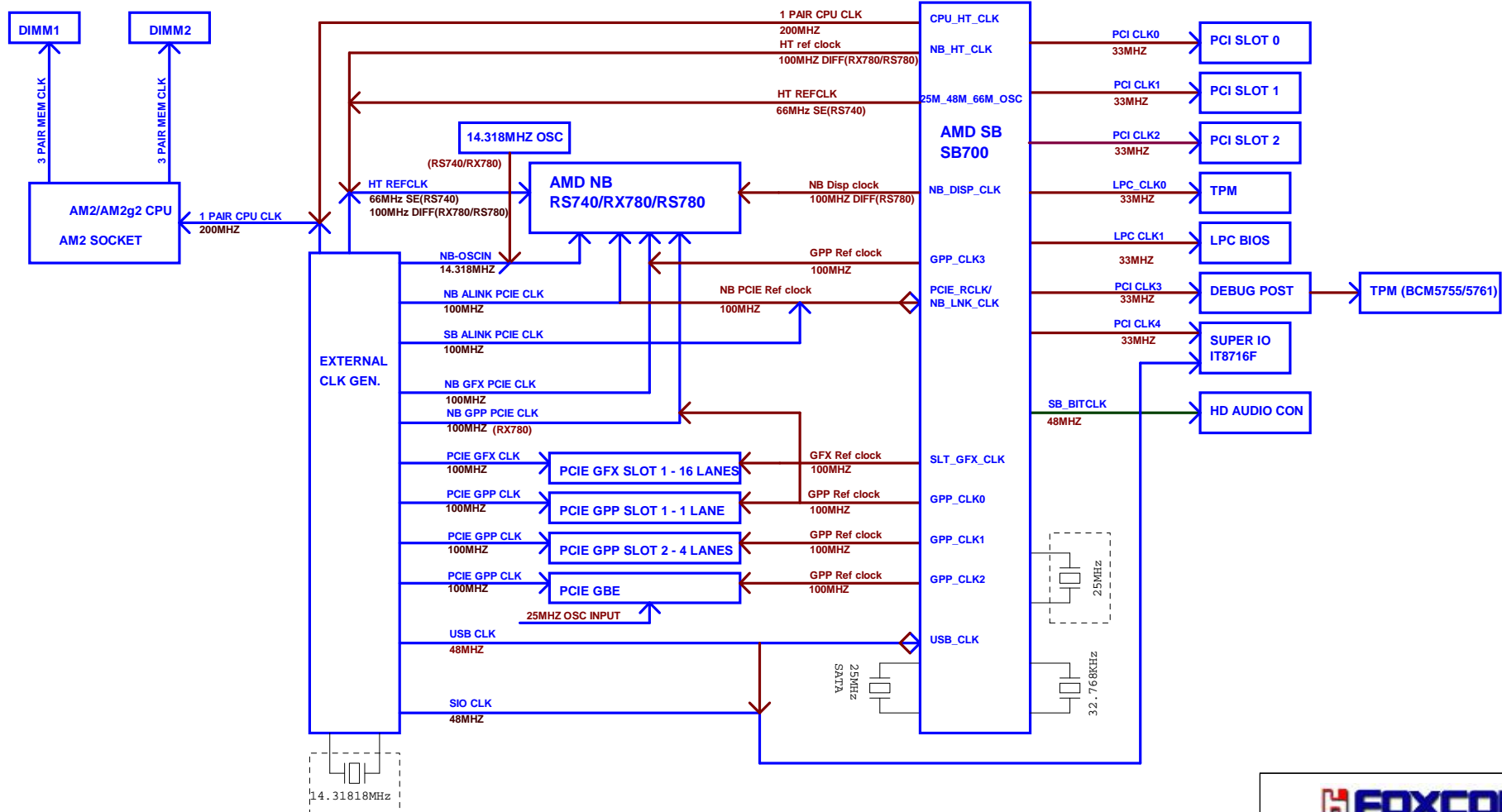
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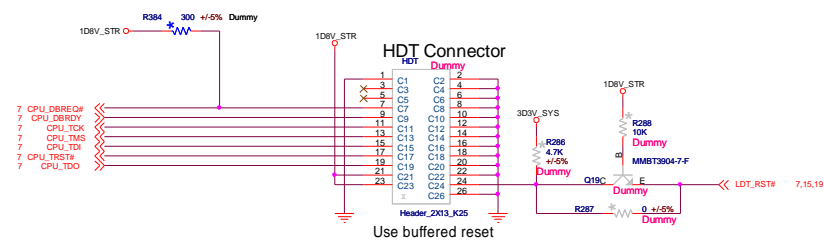
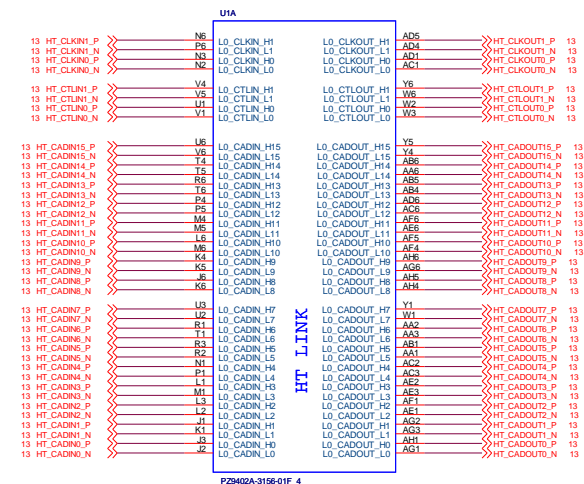
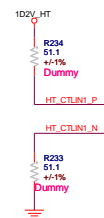
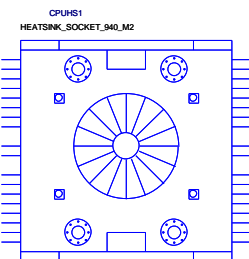
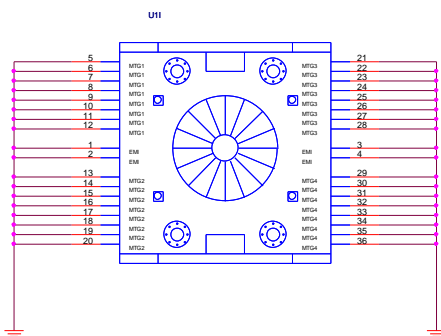
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Title			
POWER DELIVERY CHART			
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External clock mode
Internal clock mode

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HDT Header



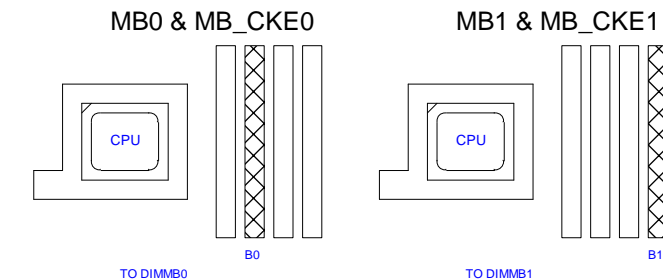
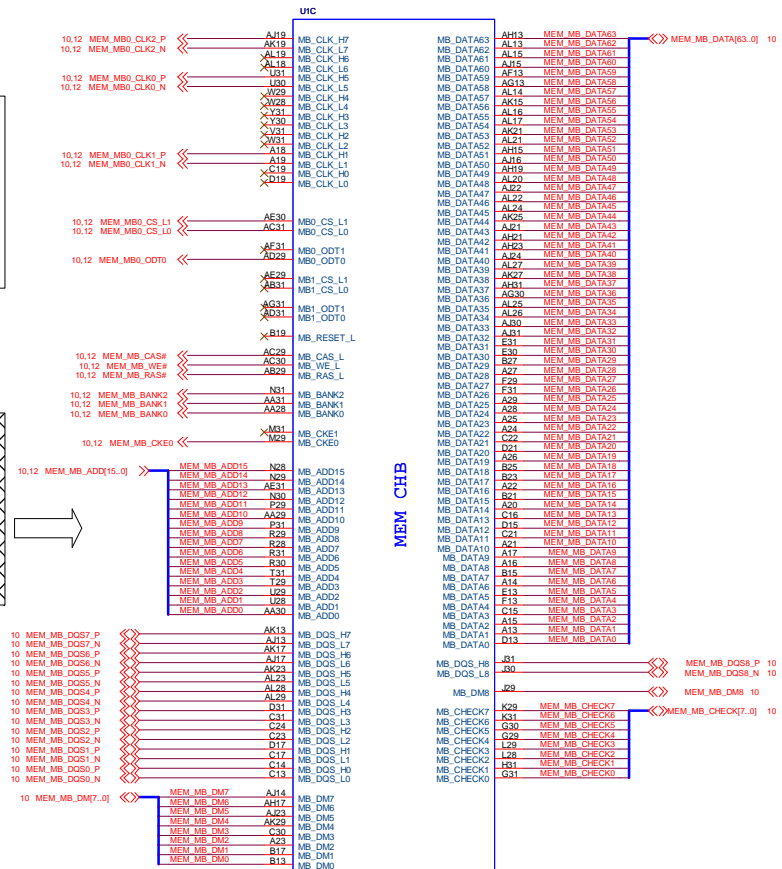
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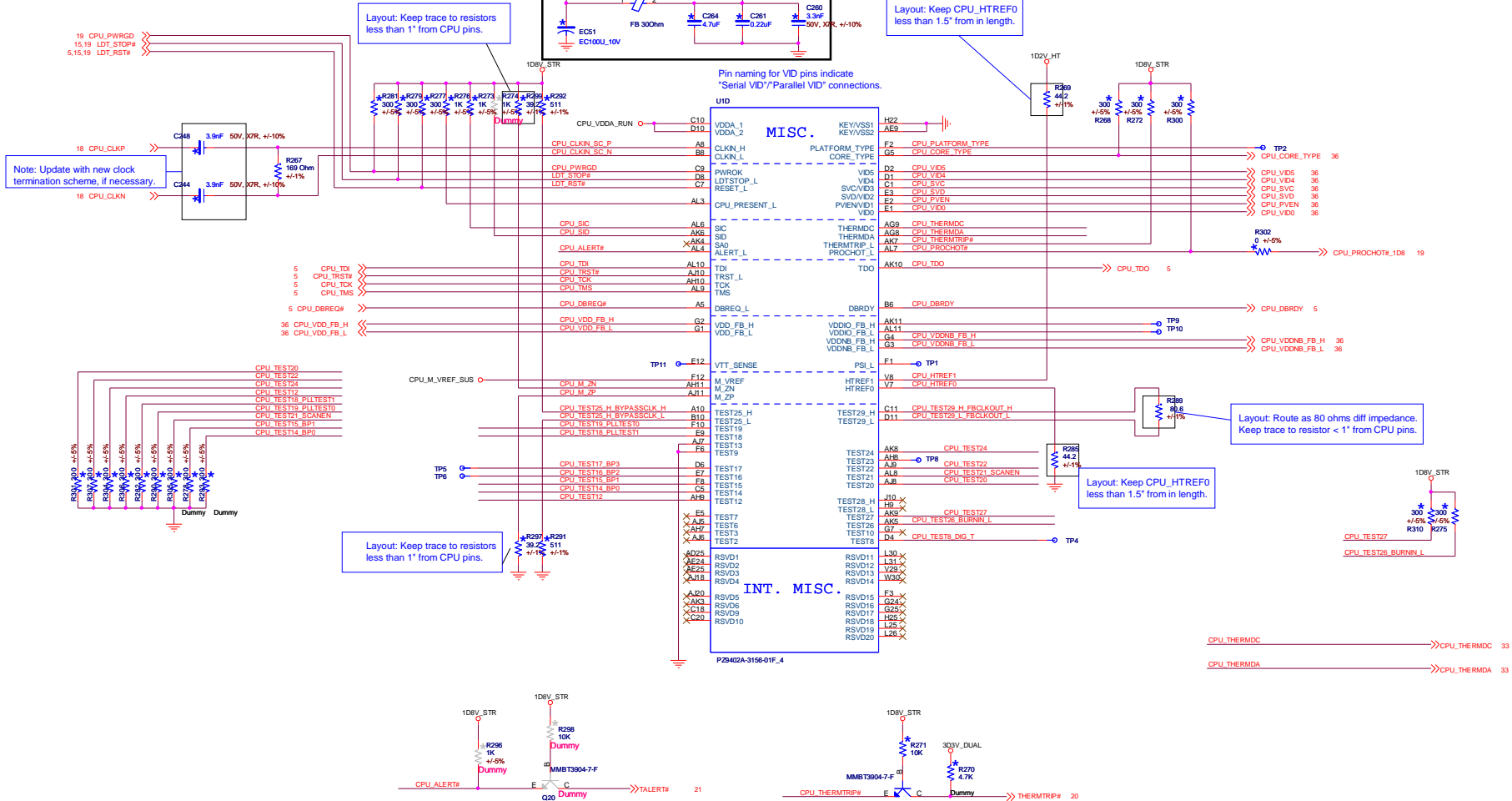
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DDR2 Memory Interface B

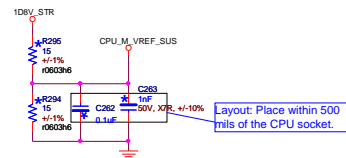


MEMORY CLOCK TRANSLATION		
DIMM	DDR2 Memory Signal	CPU Signal
DIMM A0	MEM_MAO_CLK2	MA_CLK7
	MEM_MAO_CLK1	MA_CLK1
	MEM_MAO_CLK0	MA_CLK5
DIMM A1	MEM_MAI_CLK2	MA_CLK6
	MEM_MAI_CLK1	MA_CLK0
	MEM_MAI_CLK0	MA_CLK4
DIMM B0	MEM_MB0_CLK2	MB_CLK7
	MEM_MB0_CLK1	MB_CLK1
	MEM_MB0_CLK0	MB_CLK5
DIMM B1	MEM_MB1_CLK2	MB_CLK6
	MEM_MB1_CLK1	MB_CLK0
	MEM_MB1_CLK0	MB_CLK4

CPU Control and Miscellaneous



CPU_M_VREF_SUS

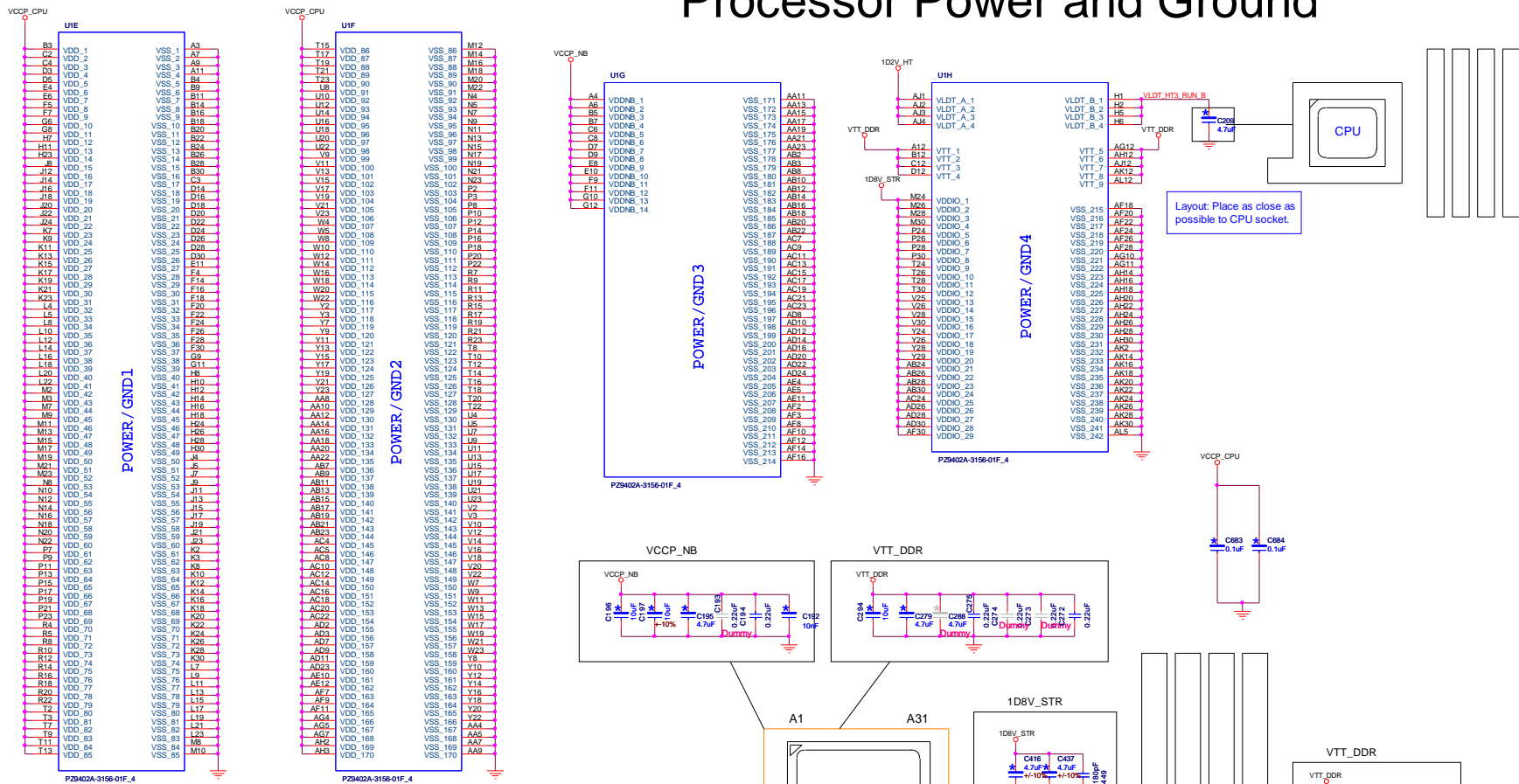
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Title	CPU CONTROL & MISC
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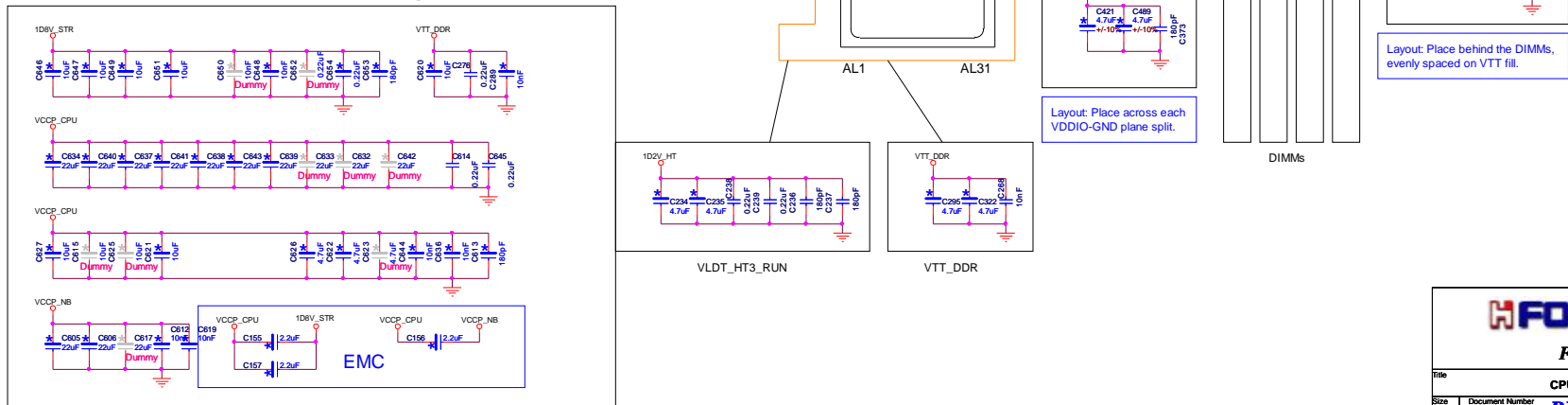
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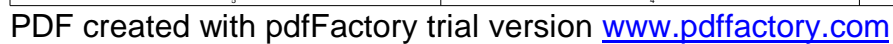
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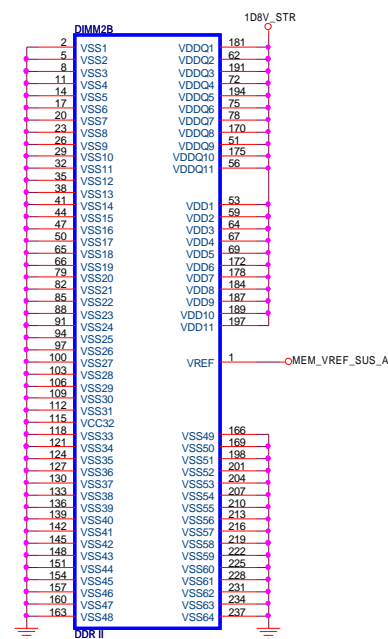
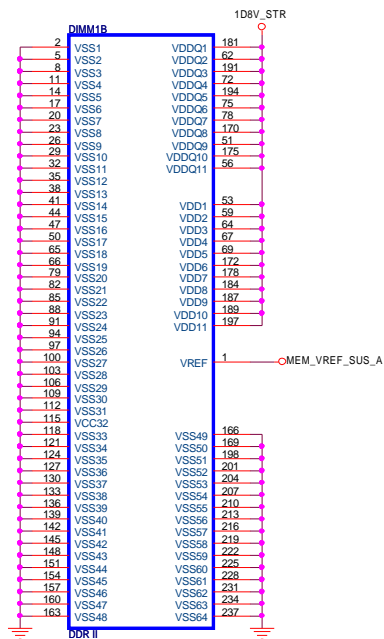
Processor Power and Ground



Bottom Side Decoupling

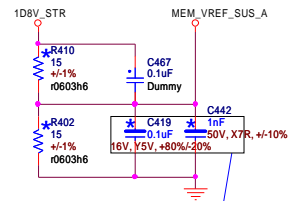






MEM_VREF_SUS

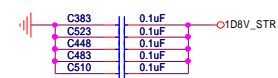
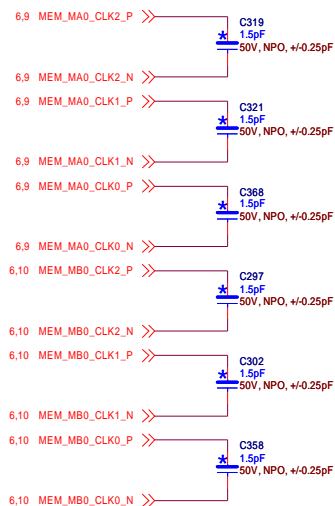
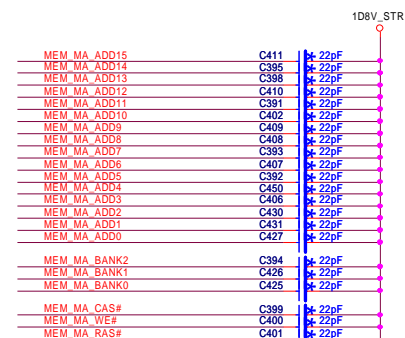
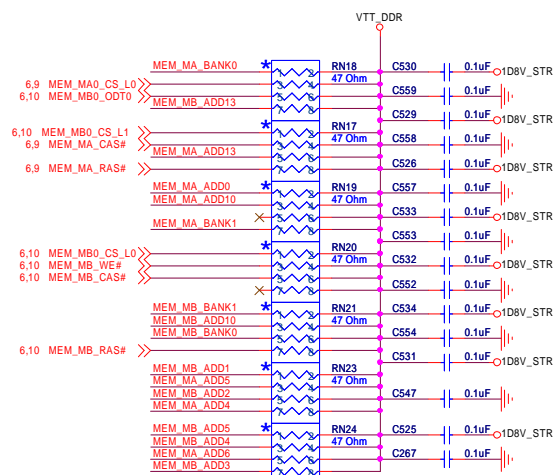
MEM_VREF_SUS



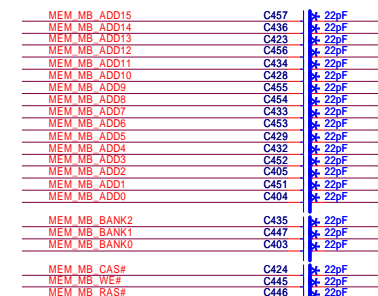
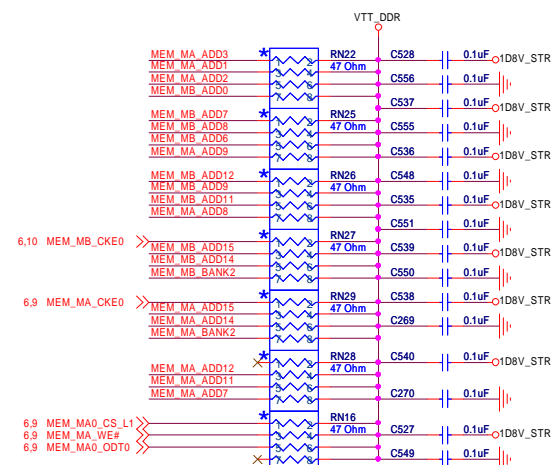
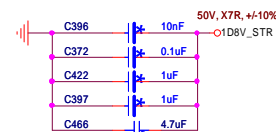
Layout: Place within 500 mils of the DIMMB1 socket.


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Title		
DDR2 DIMM POWER		
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6.9 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
 6.9 MEM_MA_BANK[2..0] >> MEM_MA_BANK[2..0]
 6.10 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
 6.10 MEM_MB_BANK[2..0] >> MEM_MB_BANK[2..0]



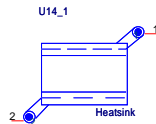
EMI decoupling cap, place evenly around 1D8V_STR





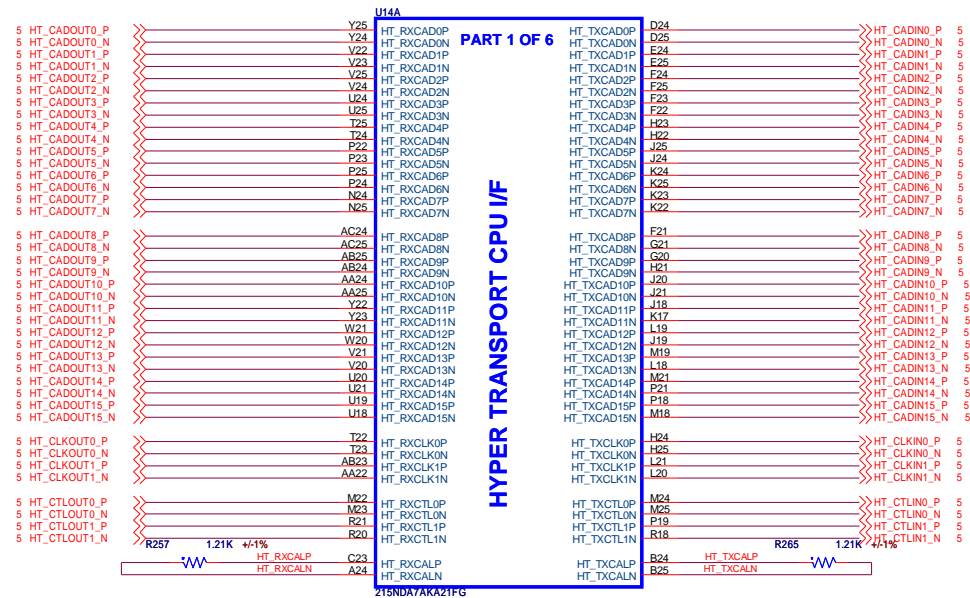
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Title			DDR2 DIMM TERMINATIONS		
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RX780/RS740/RS780 difference table (HT LINK)

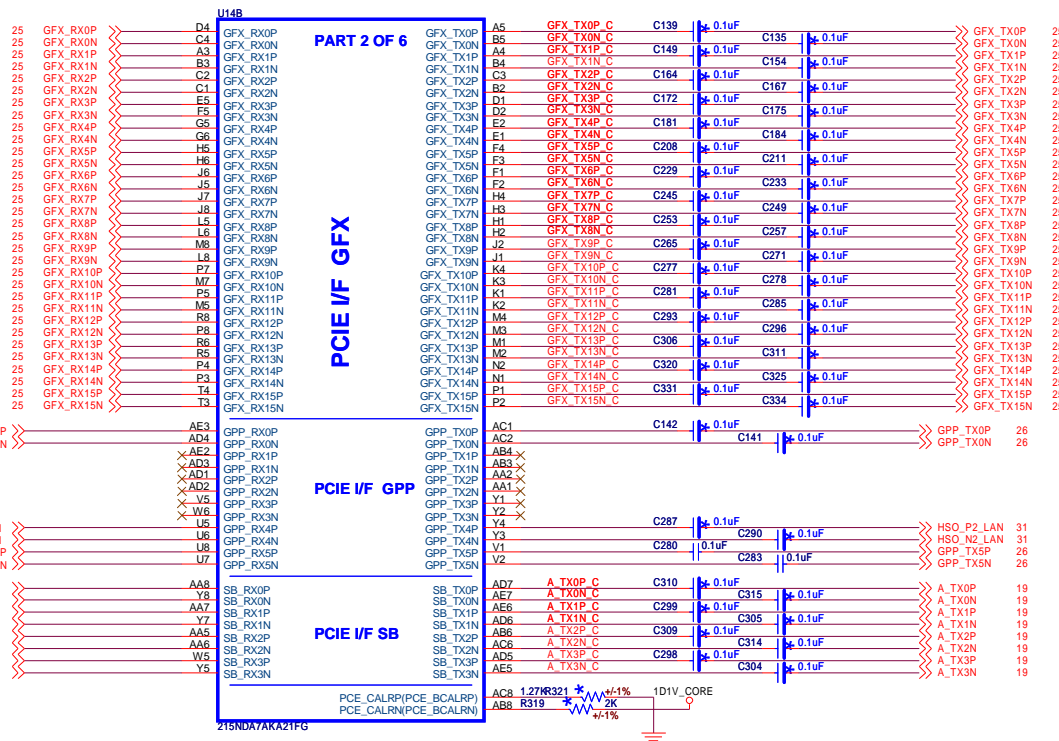
SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



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Title			RS740/RX780/RS780-HT LINK I/F
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RX780/RS740/RS780 GPP difference table

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RX780/RS740/RS780 GPP Routing table

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
SIGABIT ETHERNET	GPP3	GPP5



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Title RS740/RX780/RS780-PCIE I/F

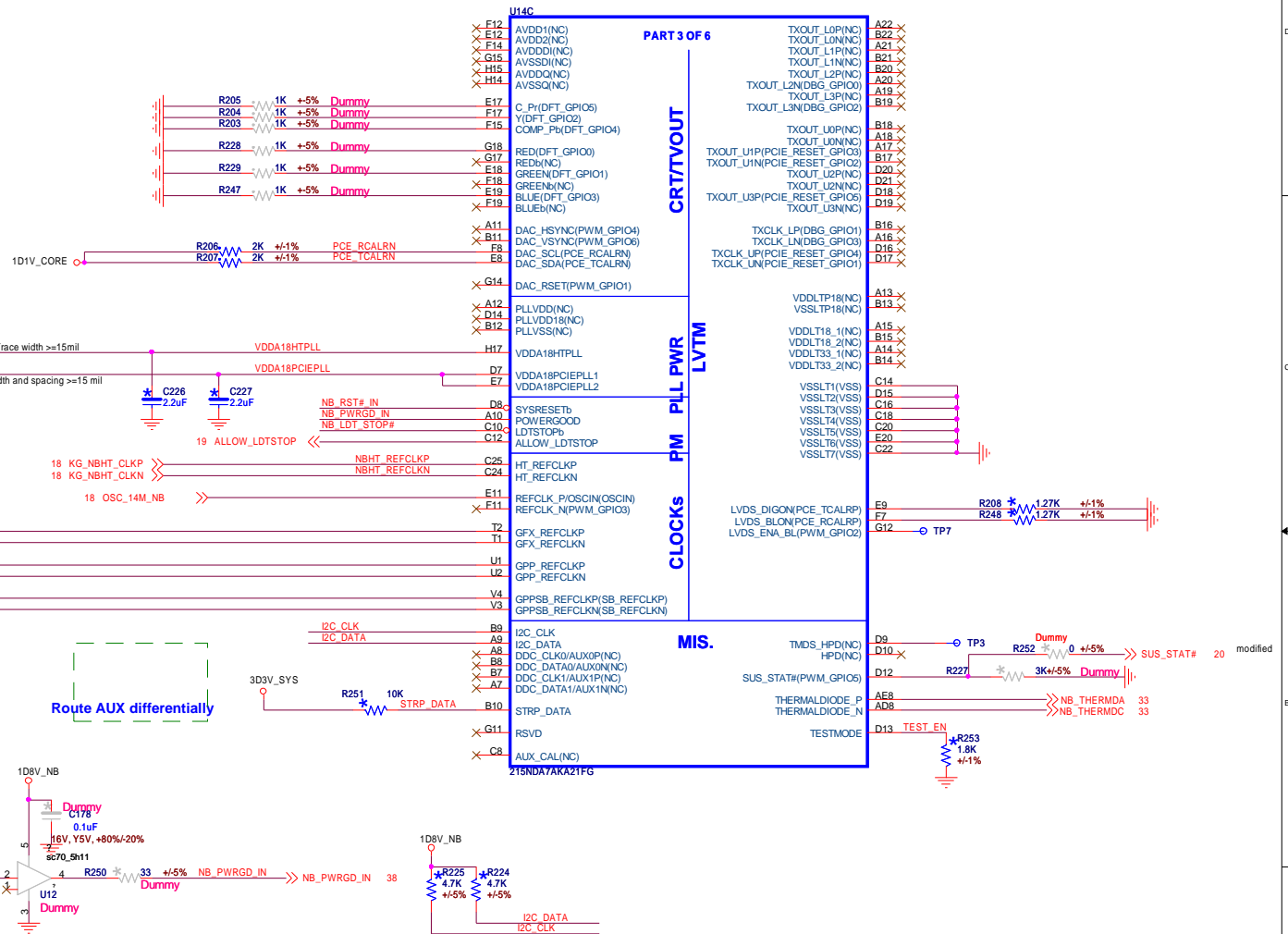
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	RS740	RX780	RS780
E17	C_Pn	DFT_GPI05	Reserved
F17	Y	DFT_GPI02	Reserved
F15	COMP_Pb	DFT_GPI04	Reserved
G18	RED	DFT_GPI00	RED
G17	REDb	NC	REDb
E18	GREEN	DFT_GPI01	GREEN
F18	GREENb	NC	GREENb
E19	BLUE	DFT_GPI03	BLUE
F19	BLUEb	NC	BLUEb
A11	HSYNC	PWM_GPI04	HSYNC
B11	VSYNc	PWM_GPI06	VSYNc
F8	DAC_SCL	PCE_RCALRN	DAC_SCL
E8	DAC_SDA	PCE_TCALRN	DAC_SDA

	RS740	RX780	RS780
C25	HT_REFCLK	HT_REFCLKP	HT_REFCLKN
C24	HT_ST_CLK	HT_REFCLKN	HT_REFCLKN
E11	OSCIN	OSCIN	REF_CLKP
F11	DFT_GPI04	PWM_GPI03	REF_CLKN
U1	Reserved	GPP_REFCLKP	GPP_REFCLKP(I)
U2	Reserved	GPP_REFCLKN	GPP_REFCLKN(I)
V4	GPSSB_REFCLKP	SB_REFCLKP	GPSSB_REFCLKP
V3	GPSSB_REFCLKN	SB_REFCLKP	GPSSB_REFCLKN

	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)IN	OD	OD	OD/3.3V IN
LDT_STOP# IN(default)OUT	3.3V IN	1.8V IN	3.3V IN/OD
SYSTEMRESETb IN	3.3V IN	1.8V IN	3.3V IN



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Address bus to debug bus mapping

TP_STRP_DB_EN

TP_DBCH_EN

TP_DB_SEL0

TP_DB_SEL1

TP_DB_SEL2

TP_DB_SEL3

TP_DB_SEL4

TP_DB_SEL5

TP_DB_MUX0

TP_DB_MUX1

TP_DB_MUX2

TP_DB_MUX3

TP_DB_MUX4

TP_DBA_OUT14

TP_DBA_OUT15

U14D

PAR 4 OF 6

MEM_A0(NC)

MEM_A1(NC)

MEM_A2(NC)

MEM_A3(NC)

MEM_A4(NC)

MEM_A5(NC)

MEM_A6(NC)

MEM_A7(NC)

MEM_A8(NC)

MEM_A9(NC)

MEM_A10(NC)

MEM_A11(NC)

MEM_A12(NC)

MEM_A13(NC)

MEM_BA0(NC)

MEM_BA1(NC)

MEM_BA2(NC)

MEM_RAS0(NC)

MEM_CAS0(NC)

MEM_WE0(NC)

MEM_CS0(NC)

MEM_CKE(NC)

MEM_ODT(NC)

MEM_CK0(NC)

MEM_CK1(NC)

MEM_COMPP0(NC)

MEM_COMPN(NC)

MEM_DQ0/DVQ_VSYN(NC)

MEM_DQ1/DVQ_HSYN(NC)

MEM_DQ2/DVQ_DE(NC)

MEM_DQ3/DVQ_D0(NC)

MEM_DQ4(NC)

MEM_DQ5/DVQ_D1(NC)

MEM_DQ6/DVQ_D2(NC)

MEM_DQ7/DVQ_D4(NC)

MEM_DQ8/DVQ_D3(NC)

MEM_DQ9/DVQ_D5(NC)

MEM_DQ10/DVQ_D6(NC)

MEM_DQ11/DVQ_D7(NC)

MEM_DQ12(NC)

MEM_DQ13/DVQ_D9(NC)

MEM_DQ14/DVQ_D10(NC)

MEM_DQ15/DVQ_D11(NC)

MEM_DQS0P/DVQ_IDCKP(NC)

MEM_DQS0N/DVQ_IDCKN(NC)

MEM_DQS1P(NC)

MEM_DQS1N(NC)

MEM_DM0(NC)

MEM_DM1/DVQ_D8(NC)

IOPLLVD18(NC)

IOPLLVD1(NC)

IOPLLVSS(NC)

MEM_VREF(NC)

AA18

AA20

AA19

Y19

V17

AA17

AA15

Y16

AC20

AD19

AE22

AC18

AB20

AD22

AC22

AD21

Y17

W18

AD23

AE24

W17

AE19

AE23

AE24

AD23

AE18

SBD_MEM/DVQ_I/F

218NDAYAKA21FG

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Note: for RS780, change R294 to 150R as AUX_CAL, place close to pin C8

Note: for RX780, R320 (RX780_DFT_GPIO1) to 3K accordingly

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740: pin DFT_GPIO1

RX780: pin DFT_GPIO1

RS780: pin SUS_STAT#

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Note: for RX780, strap resistor is R432

Enables the Test Debug Bus using GPIO and/or memory IO

1 : Disable (RS740); Enable (RX780/RS780)

0 : Enable (RS740); Disable(RX780/RS780)

RS740: pin DFT_GPIO5

RX780: pin DFT_GPIO5

RS780: pin VSYNC

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Note: for RX780, strap resistor is R458,R452,R327

Enables Side port memory

1. Disable (RS740/RS780)

0 : Enable (RS740/RS780)

RS740: pin DFT_GPIO0

RS780: pin HSYN

RX780: Not Applicable

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

Note: for RX780, change following pull-down resistor to 3K accordingly

R324(RX780_DFT_GPIO0)

Enables Test debug bus using PCIE bus

1. Disable (can be enabled thru nbcfg register)

0 : Enable

RX780: pin DFT_GPIO0

RS780: configurable thru register setting only

RS740: Not supported

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

These pin straps are used to configure PCI-E GPP mode.

111: register defined (register default to Config E) default

110: 4-0-0-0-0 Config A

101: 4-4-0-0-0 Config B

100: 4-2-2-0-0 Config C

011: 4-2-1-1-0 Config D

010: 4-1-1-1-1 Config E

others: register defined (default to Config E)

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

Note: for RX780, strap resistor is R458,R452,R327

111: 1-1-1-1-1-1 Mode L default

110: 1-1-1-1-1-1 Mode L

101: 2-0-2-0-2-0 Mode C2

100: 2-0-2-0-1-1 Mode K

011: 2-0-1-1-1-1 Mode E

010: 1-1-1-1-1-1 Mode L

001: 4-0-0-0-1-1 Mode C

000: 4-0-0-0-2-0 Mode B

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

Note: No HW strap

1-1-1-1-1-1 Mode L default

1-1-1-1-1-1 Mode L

2-0-2-0-2-0 Mode C2

2-0-2-0-1-1 Mode K

2-0-1-1-1-1 Mode E

1-1-1-1-1-1 Mode L

4-0-0-0-1-1 Mode C

4-0-0-0-2-0 Mode B

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Title

RS740/RX780/RS780-SPMEM/STRAPS

Size

Document Number

RX780

Rev

A

Date

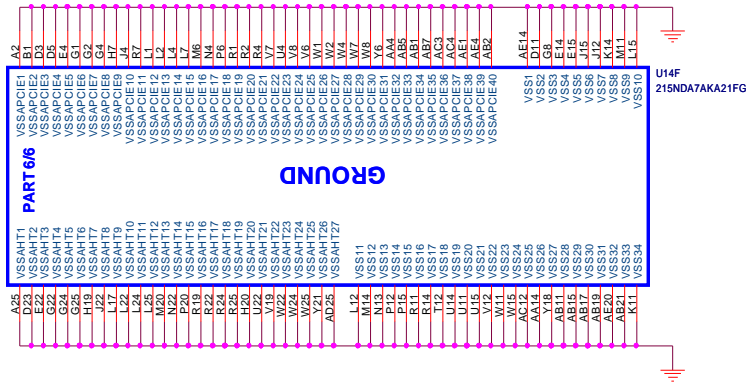
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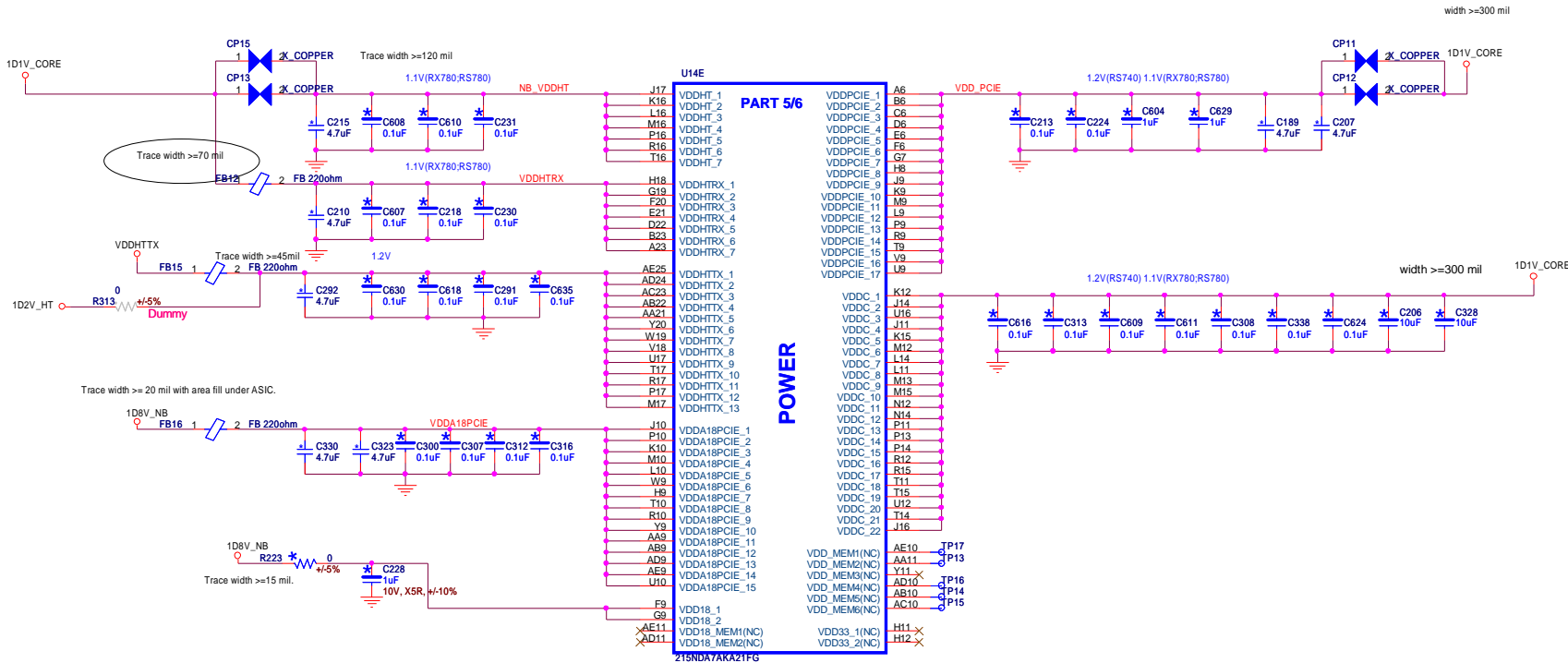
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.8V(DDR3)	VDDLT18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC




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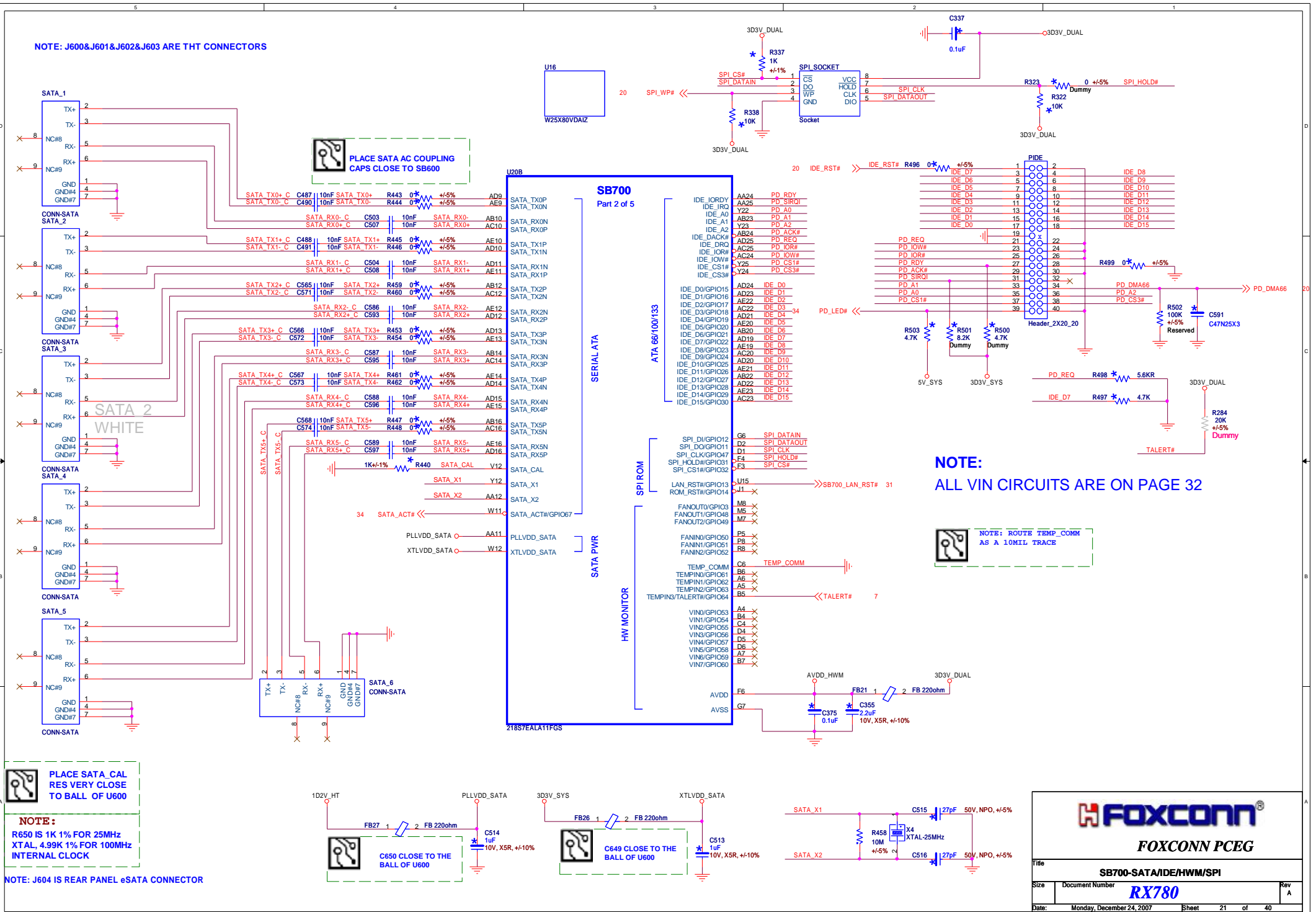




	GPIO41	GPIO40	GPIO39	GPIO38	NB	EXT_CLK	GIGABIT	DVI	HDMI
J	1	0	0	0			TBD		
K	1	0	0	1			TBD		
L	1	0	1	0			TBD		
M	1	0	1	1			TBD		
N	1	1	0	0			TBD		
P	1	1	0	1			TBD		
R	1	1	1	0			TBD		
S	1	1	1	1			TBD		

				A
<p align="center">FOXCONN PCEG</p>				
Title				
<p align="center">SB700-ACPI/GPIO/USB/AUDIO</p>				
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NOTE: J600&J601&J602&J603 ARE THT CONNECTORS

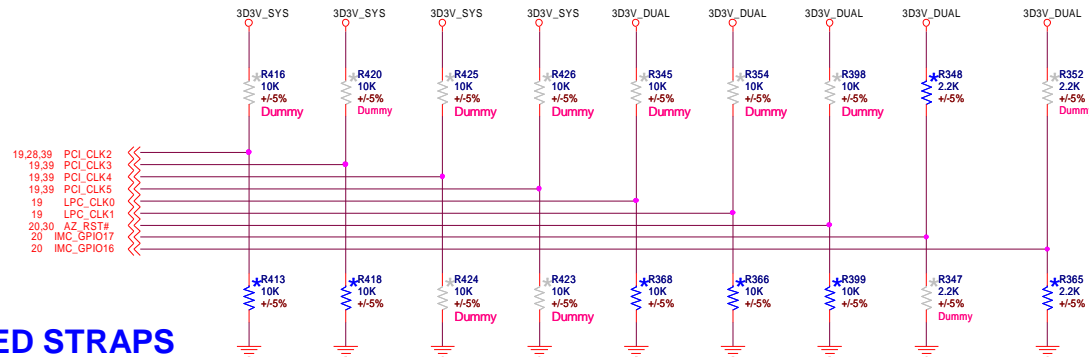


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Title			SB700-SATA/IDE/HWM/SPI
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NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



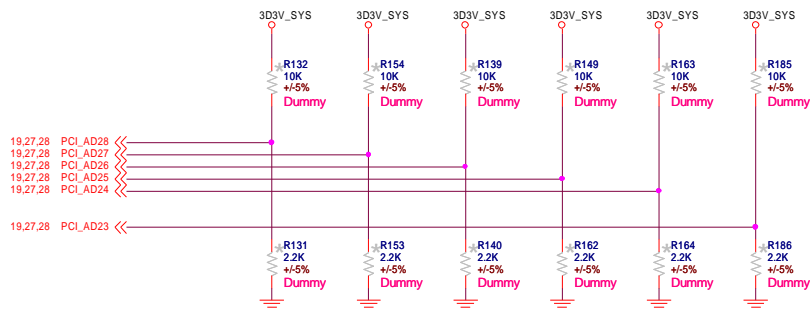
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT		L, H = LPC ROM L, L = FWH ROM

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]




	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

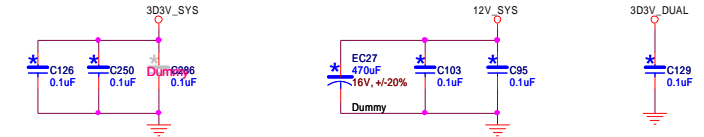
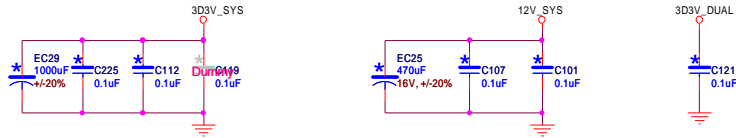
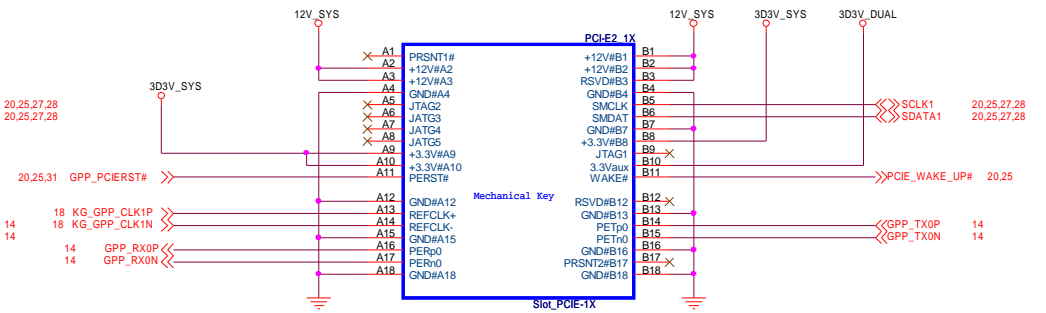
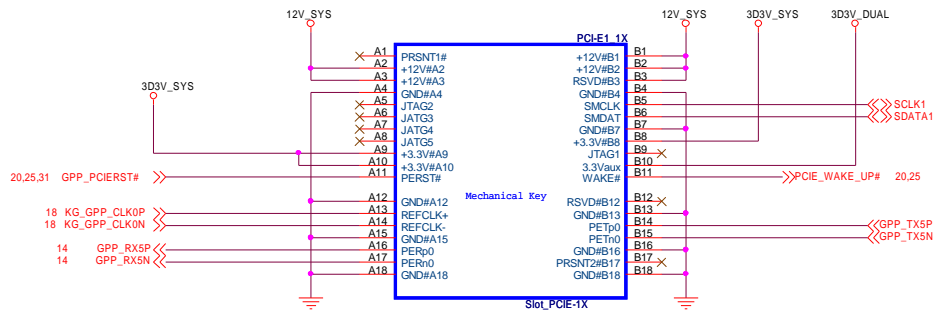
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	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

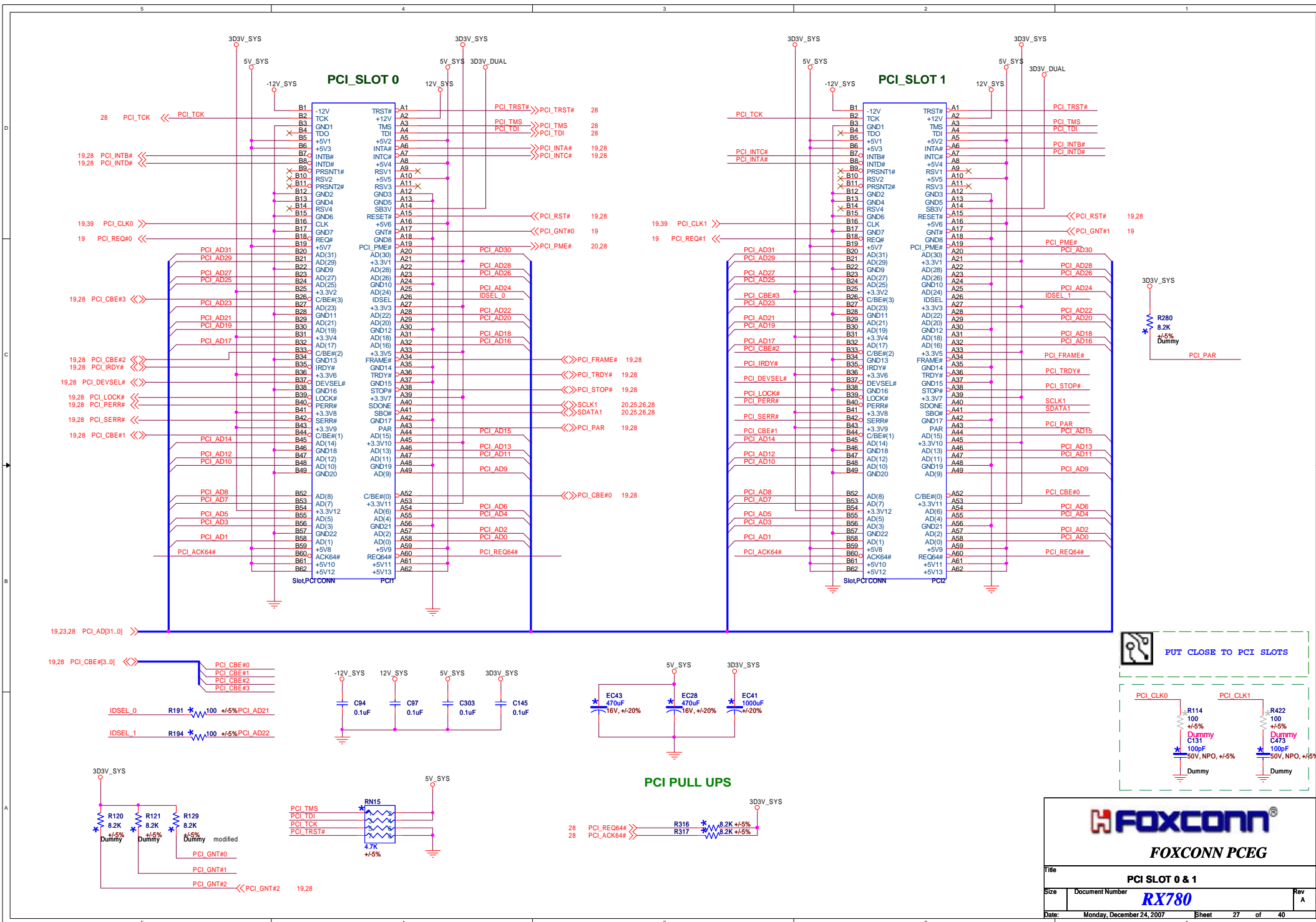
		
FOXCONN PCEG		
Title CRT & TVOUT		
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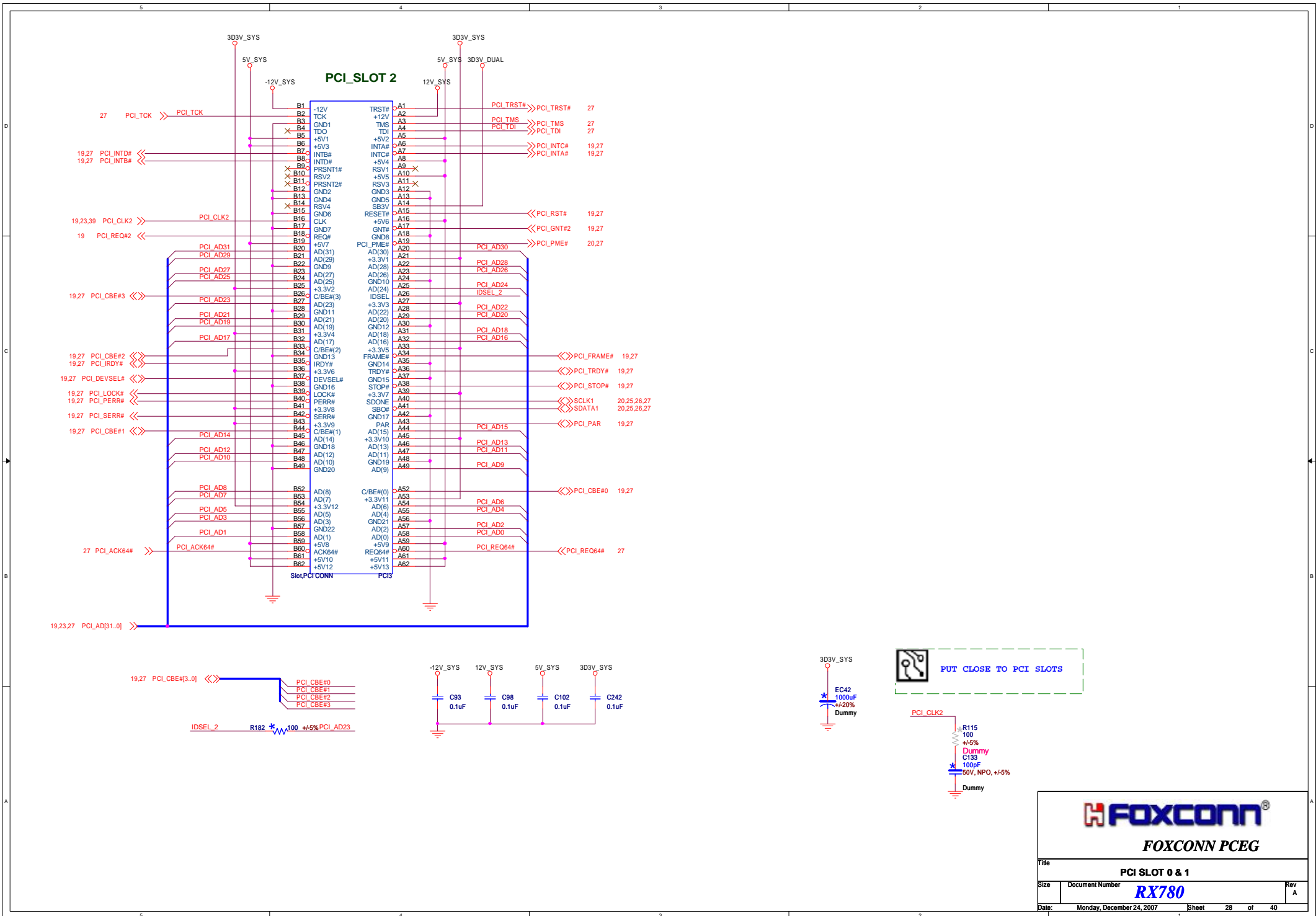


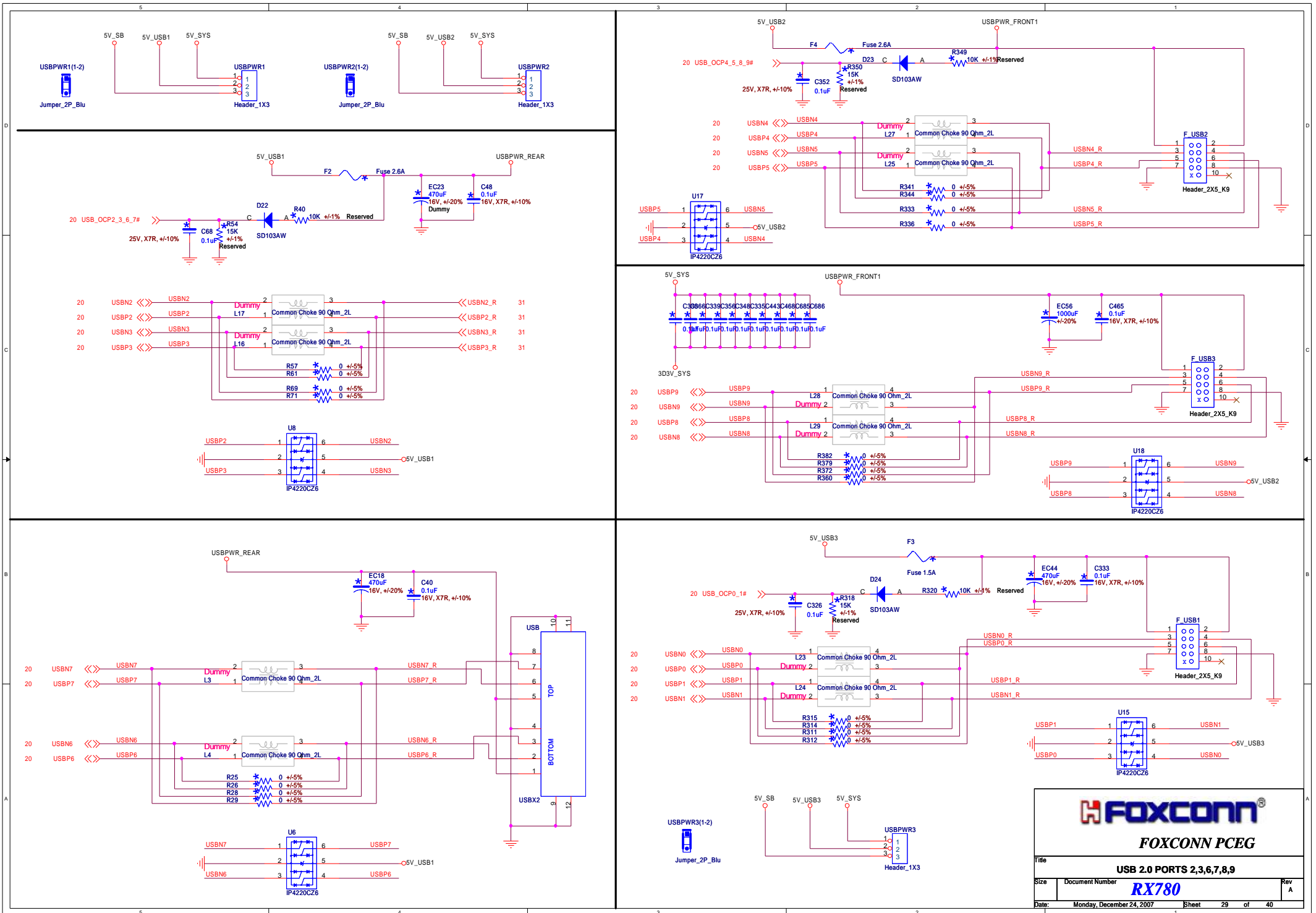
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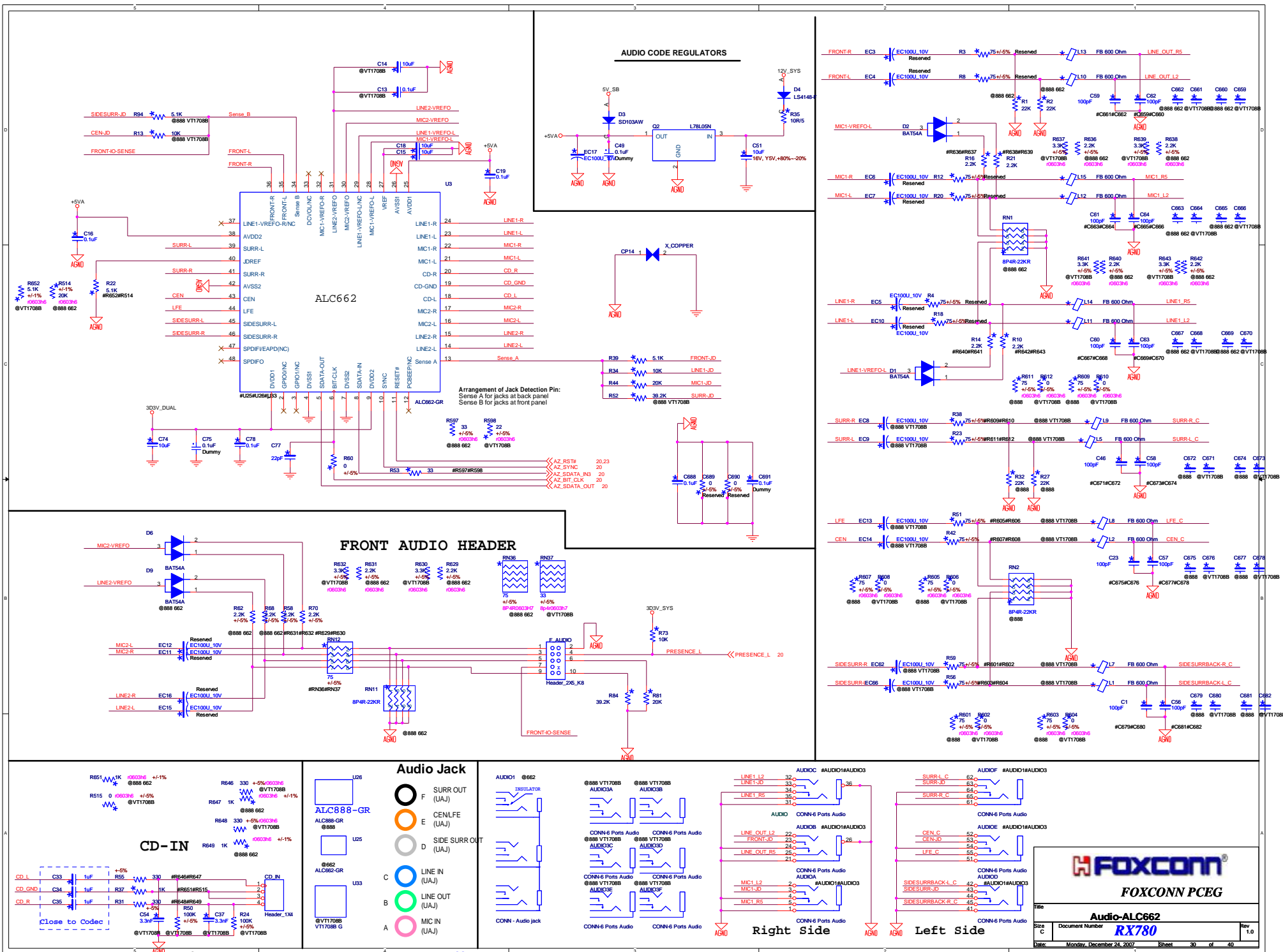
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Title			PCIE x1 & PCI SLOT 2
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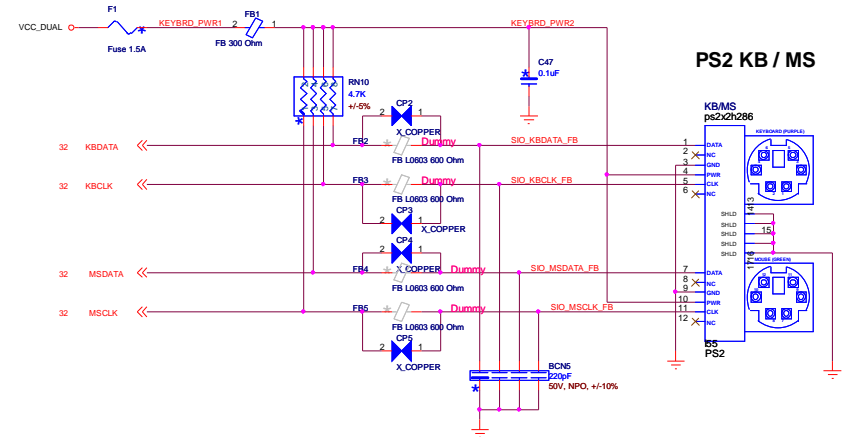
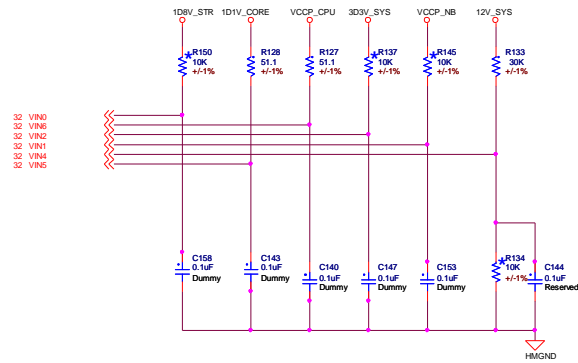






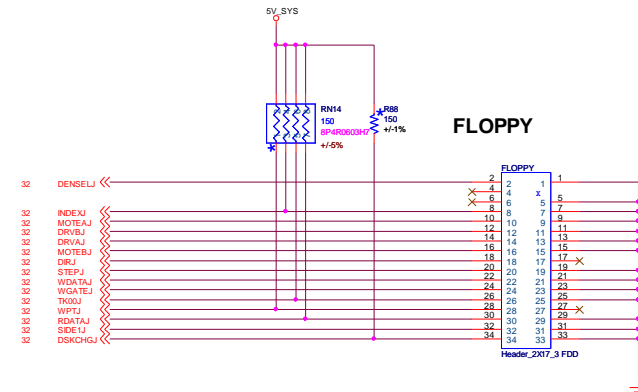
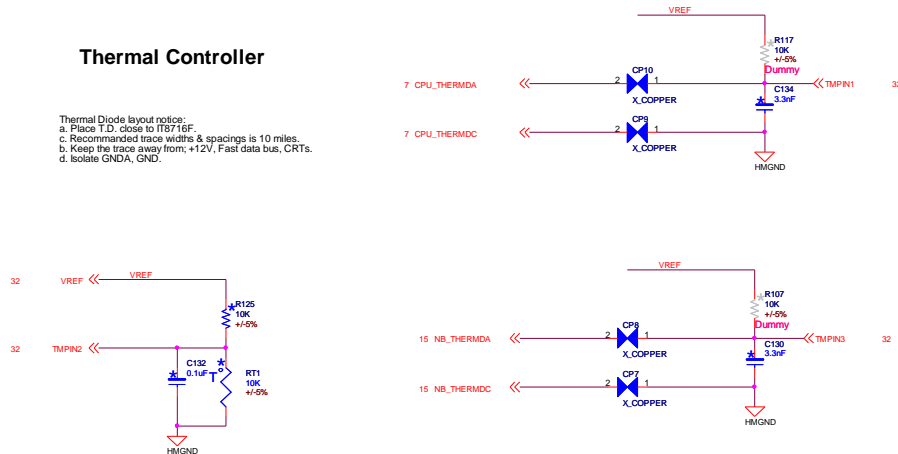


Voltage Monitor



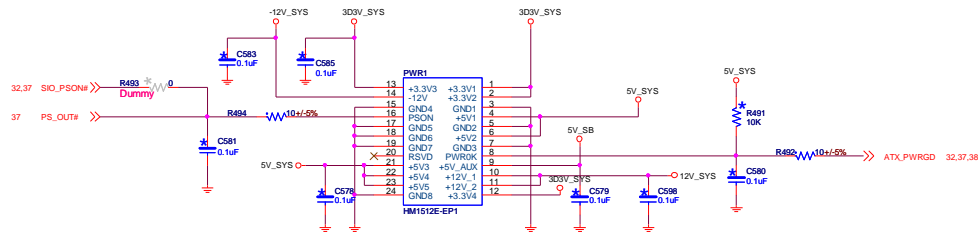
Thermal Controller

Thermal Diode layout notice:
a. Place T.D. close to I18716F.
b. Keep the trace away from; +12V, Fast data bus, CRTs.
c. Recommended trace width & spacings is 10 mils.
d. Isolate GND, GND.

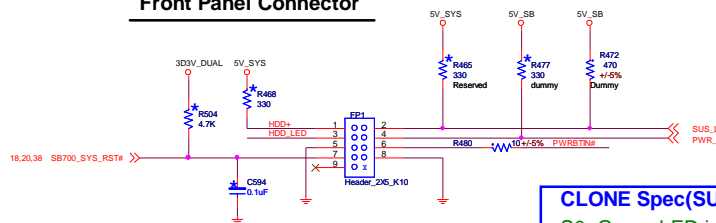


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ATX Connector



Front Panel Connector

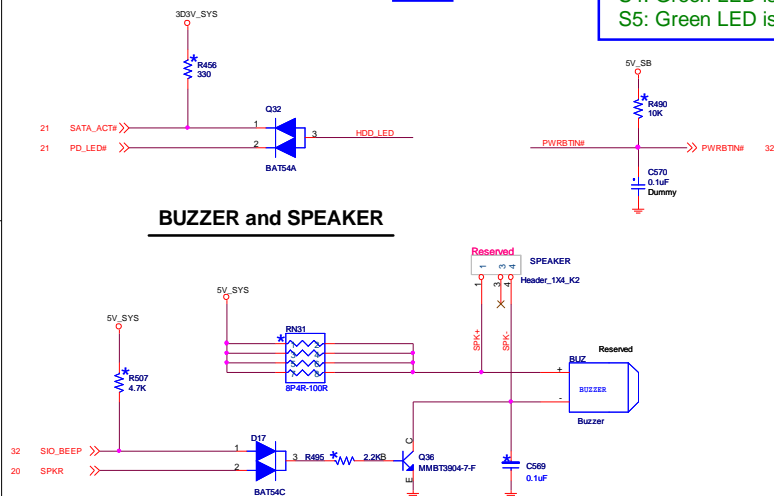


CLONE Spec(SUS_LED only)

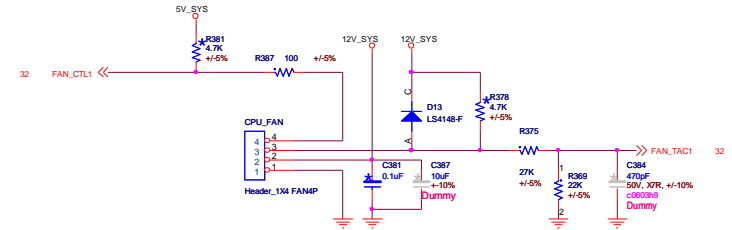
S0: Green LED is on;
S1: Green LED is blinking;
S3: Green LED is off;
S4: Green LED is off;
S5: Green LED is off.

Pin	Signal
1	FP PWR/SLP
2	FP PWR/SLP
3	FP PWR/SLP
4	FP PWR/SLP
5	FP PWR/SLP
6	FP PWR/SLP
7	FP PWR/SLP
8	FP PWR/SLP
9	FP PWR/SLP
10	FP PWR/SLP

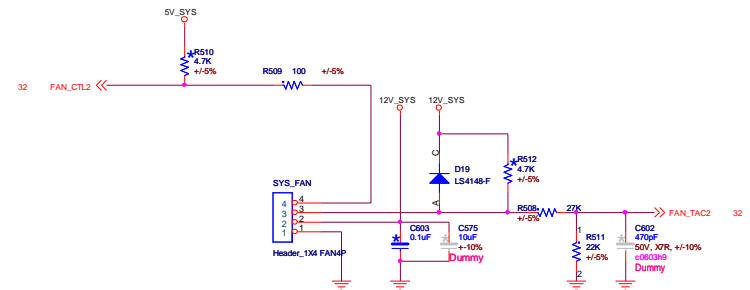
BUZZER and SPEAKER



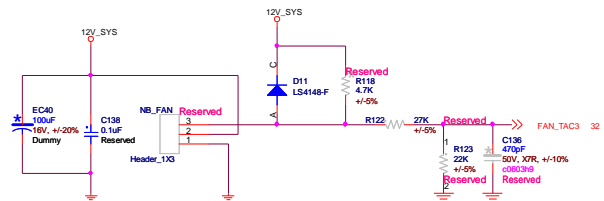
CPU FAN



SYS FAN



NB FAN



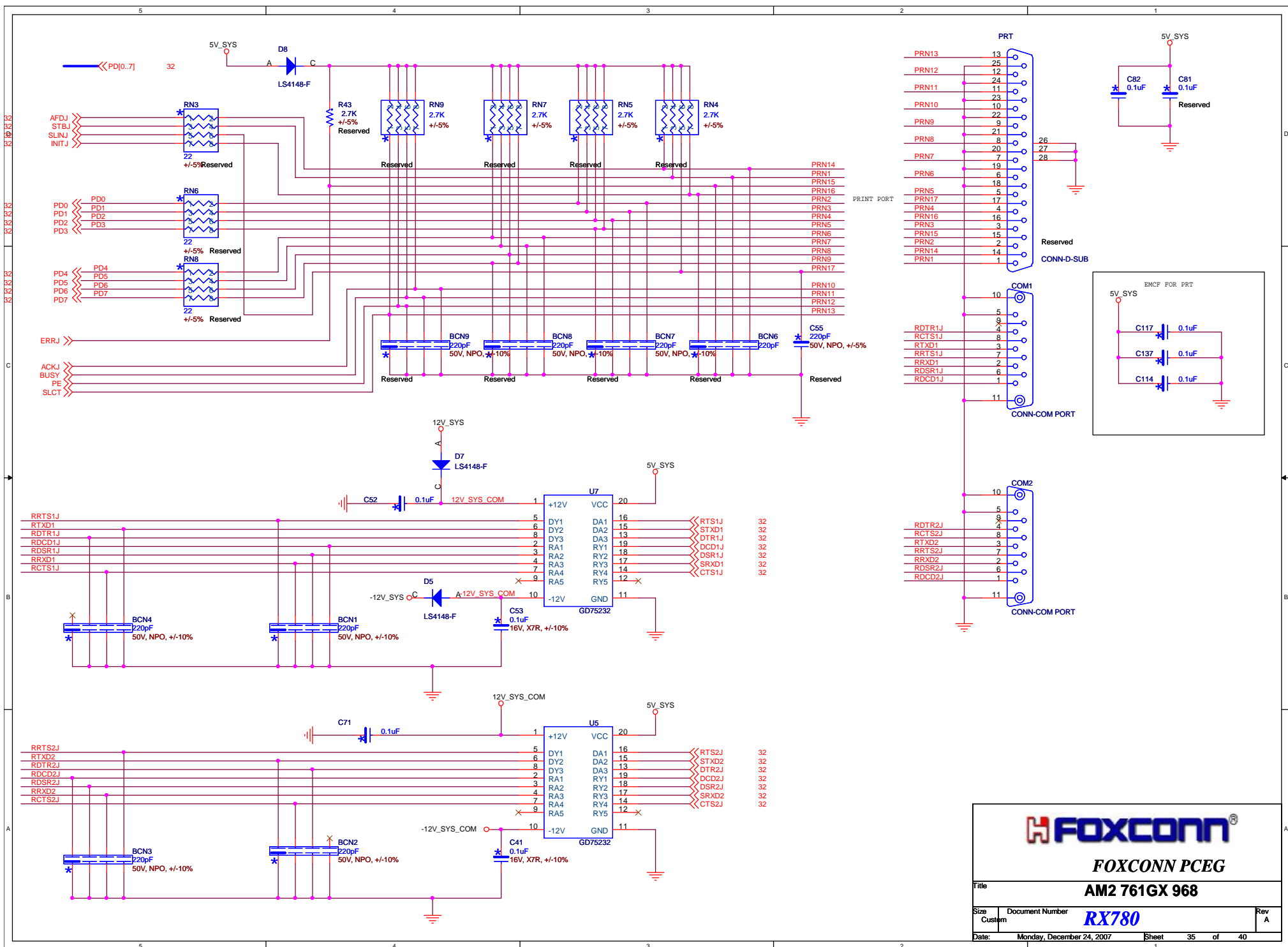
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ATX/Front Panel/Fan CTRL

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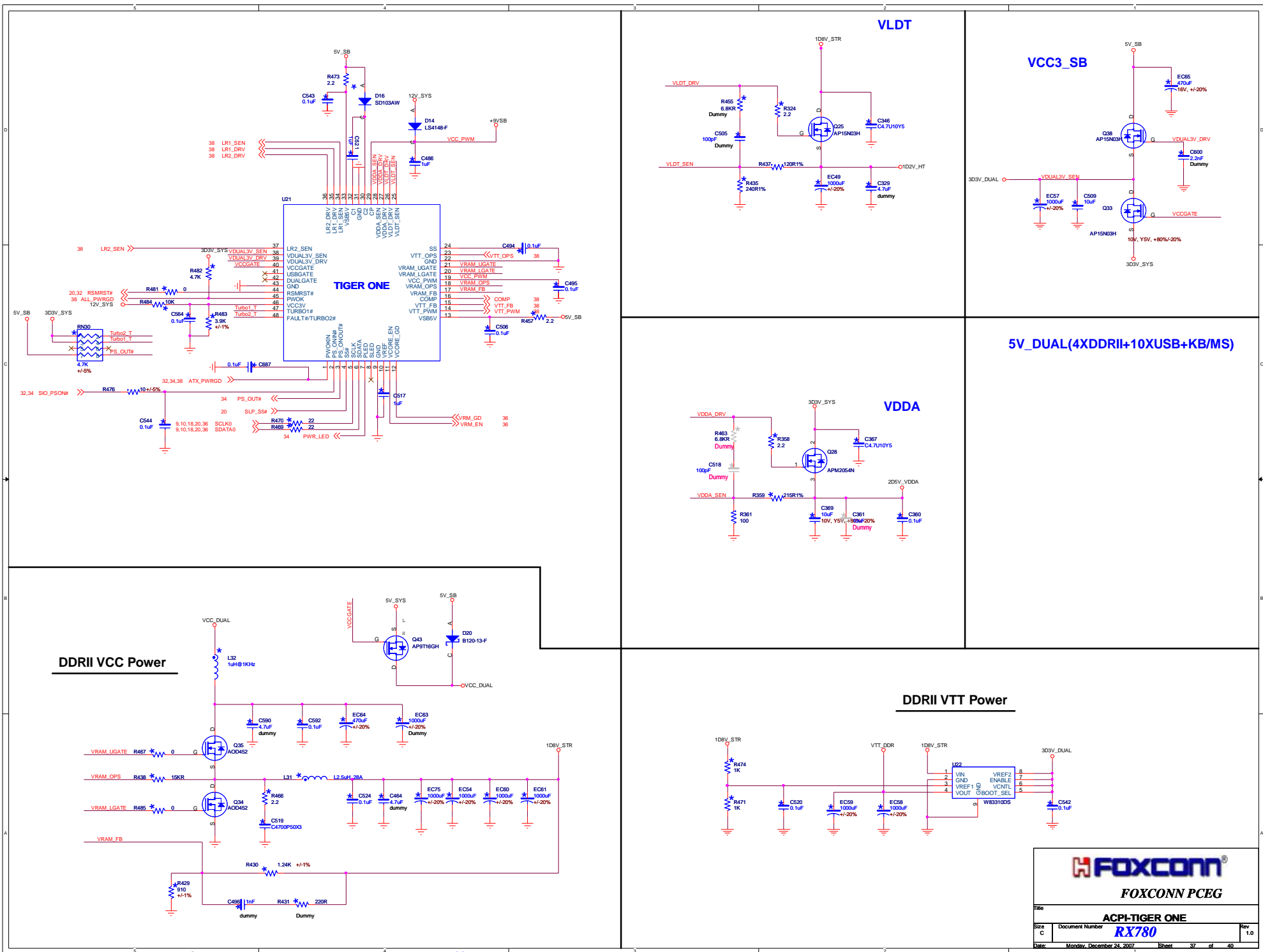




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AM2 761GX 968

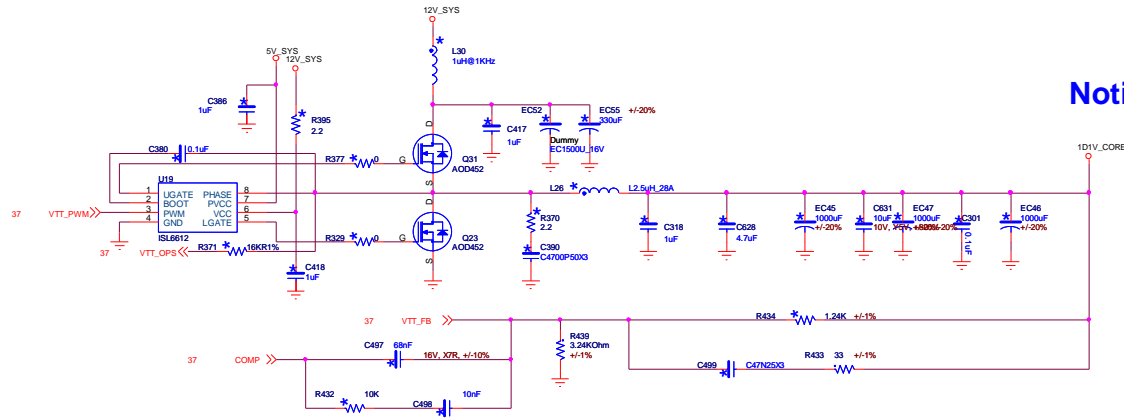
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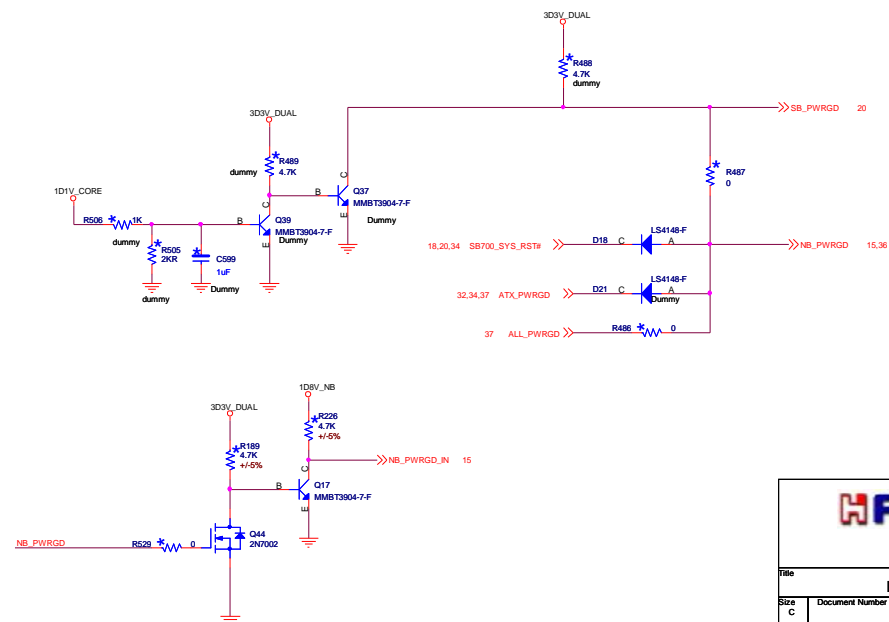
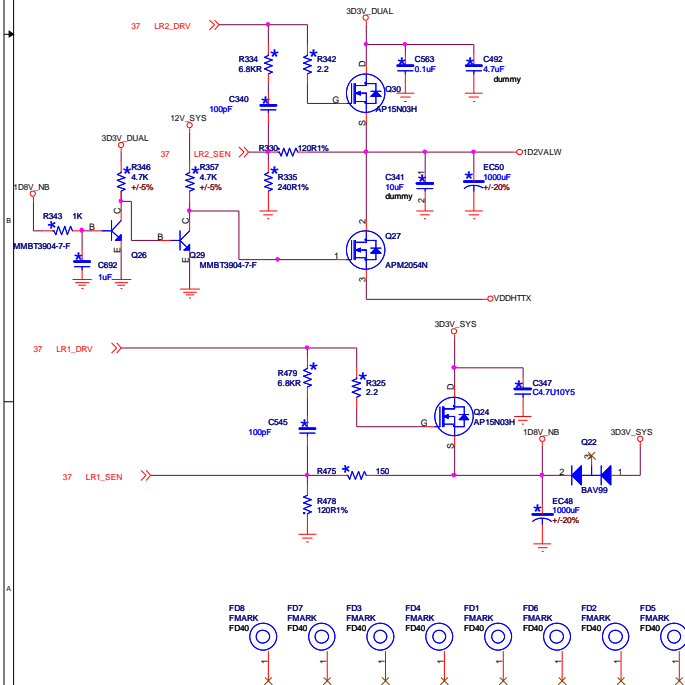
1.1V @3A FOR RX780/RS780
1.2V @2A FOR RS740

1D1V_CORE_NB Regulator

Notice layout

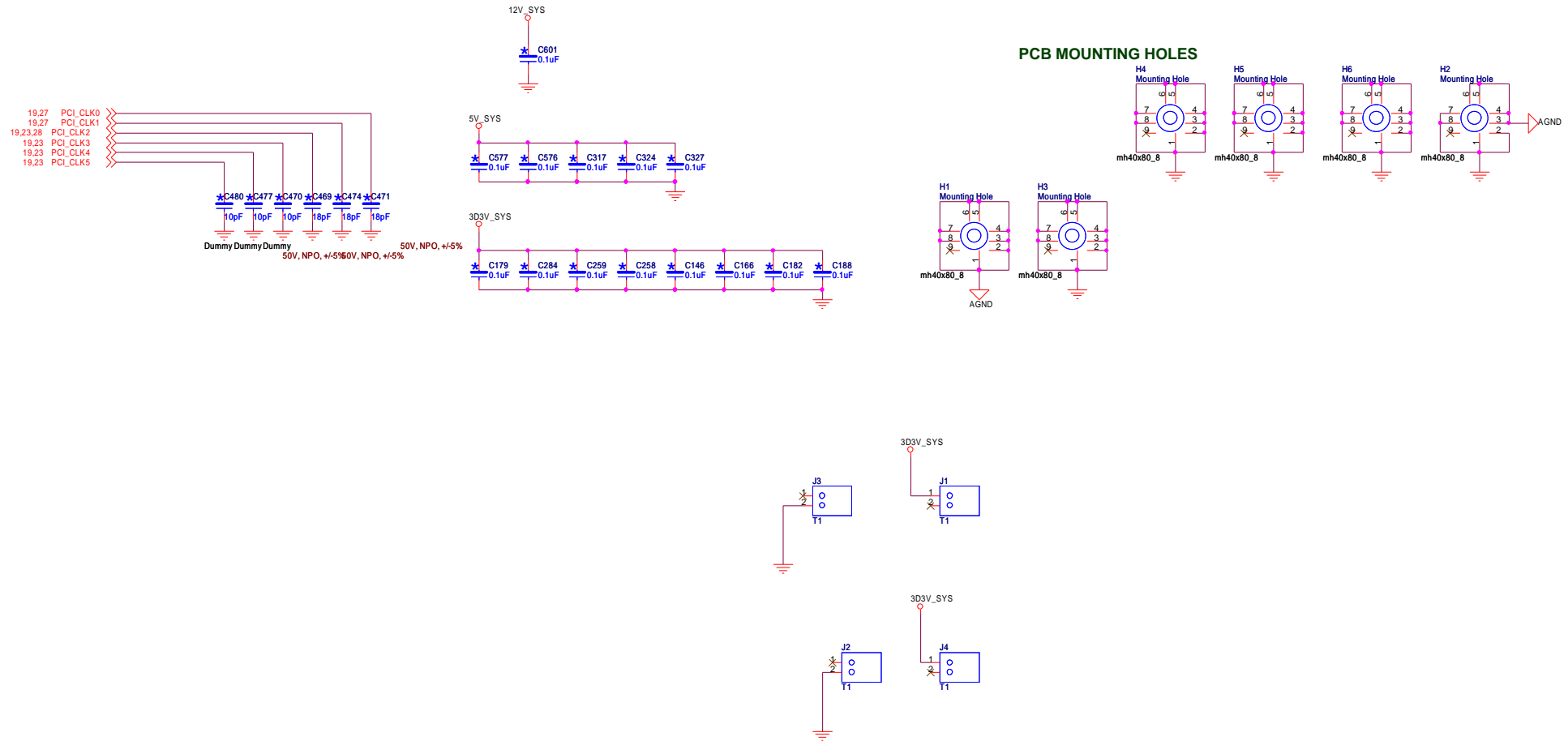


NB & SB Power Good Circuit



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NB/SB Core Power		
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FOR EMI ISSUE



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Daily Change List:

12/01/2007

- 1.Change C362,C363 from 18pf to 12pf.
- 2.Change SIO_THERM_UP from Pin Y19 to Pin G5
- 3.Change C515,C516 from 10pf to 27pf
- 4.A.DD:Q40,Q41,Q42,R403,R411,R526,C694,D22,D23,D24 For 1.2V_JHT Power sequence
- 5.Reserved R348
- 6.Add D22,D23,D24 For USB OC issue
- 7.Audio chane
- 8.Reserved C83,C85
- 9.CPU Power change
 - R244 40.2Kohm change to 43Koh
 - R181 50hm change to 510ohm
 - R231 1Kohm change to 1.6Kohm
 - R232 1Kohm change to 1.6Kohm
 - change R263 12.7Kohm to 5.2Kohm
 - change R562 13.3Kohm to 7.5Kohm
 - add 0.1uF cap 3/R244 并置
- 10.Change Q44 to 2N7002
- 11.Add C686,C696,C697,C698 (Dummy) for SMBUS
- 12.Add EC75 for 1.8V_STR Power
- 13.Add R527,R528 Delete R594
- 14.Dummy R331 ,Reserved R332
- 15.Add R529

- 08/21/2007
- (1) ON P42, R3841 change 22k
 - (2) ON P07, active R193
 - (3) ON P32,Remove R3882 and add C3510
 - (4) ON P32, add R3882 8.2k pull down Pin 33
 - (5) ON P32, change R3085 to 4.7k, and dummy R3085
 - (6) ON P43, remove R3089 R3857, R3856, C3032
 - (7) ON P35, add F1505
 - (8) ON P32, make R3085 Dummy
 - (9) ON P15, remove R2441 remove pull down).
 - (10) The R3880/R3879 resistor net work should connect to 5524's pin 102 (left side of R3091) instead of the right side R3091
 - (11) The R296/R148 resistor net work should connect to 5524's pin 112 (left side of R3092) instead of the right side R3092
 - (12) Add net SDATA2, and SCLK2
 - (13) Reconnect net SDATA1, and SCLK1


- 08/22/2007
- (1) ON P31, remove all connection to Pin D11, include R1314 and C1304.
 - (2) ON P31, Remove R421
 - (3) ON P31, Remove TP207
 - (4) ON P31, add R6, R8, R10, R11, dummy for 5754, activate for 5761.
 - (5) ON P31, add C135, C136, C139, C141, C142, C143, C191, C196, but dummy first, only use them if EMI issue required.
 - (6) ON 11, add second set memory reference.
 - (7) ON 40, connect R2638 to CPU_VDDA_RUN, instead of VDDA_RUN_OUT

- 08/23/2007
- (1) ON P20, Dummy R716
 - (2) ON P44, add EMI required capacitors
 - (3) ON P32, add two stitch cap c24, c25 for 12v and 5v plane
 - (4) ON P32, add two stitch cap c50, c88 for 12v and 3.3v plane

- 08/24/2007
- (1) ON P31, Dummy B1308, B1310, B1311

- 08/26/2007
- (1) ON P35, on component PRT, nc Pin 26
 - (1) ON P43, disconnect component H3 to grid

- 08/27/2007
- (1) ON P6, add retention module- Fan_holder, u3514
 - (1) ON P44, remove C105, C127
 - (3) ON P45, remove cp5, add R82, and R83



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CHANGE LIST		
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